METHOD FOR MAKING THREE DIMENSIONAL CIRCUIT INTEGRATION

FIELD OF THE INVENTION

The present invention relates to semiconductor circuit integration and, in particular, to a method for interconnecting, through high density micro-post wiring, multiple wafers of silicon with wire lengths of a millimeter or less. The present invention is a cost efficient method that is especially useful in high speed, high density, and low latency interconnection of circuits for providing interconnects between separately processed wafers.

PRIOR ART

In semiconductor manufacturing, reduction in device size is used to increase the density of the devices. Device scaling, however, has its limits and the cost for implementing existing technology is escalating. As device density increases, wiring has become a strong obstacle to performance and function integration. Another limitation arises from the need to interconnect circuits over wide bandwidth buses. Some examples of this include: interconnects between slow and fast memory devices, between memory and processors, and between switches and processors. Additional wiring problems also arise in applications that require interconnection of devices and structures made using widely dissimilar technologies, e.g. individual pixel addressable cameras using photodiodes and CMOS, and wireless applications with large low-loss lumped elements coupled to transistors, applications requiring interconnection of low power (CMOS) with high speed (bipolar) elements. Interconnecting separately processed wafers saves processing time and is likely to be economically efficient.

A major development in this area, particularly three-dimensional integration, was reported by J. Carson, "Emergence of stacked 3D silicon and its impact on microelectronic systems integration," Proc. of Eighth IEEE International Conference on Innovative Systems in Silicon, p.1 (1996). This paper by J. Carson is directed to stacking of fabricated and cut-up chips, such as memory chips, to create a cube. Wafers are typically 650 μm thick and 16 chips are used to form a cubic structure. Outputs to be interconnected are at the edges of the chip. The chips are interconnected and the outputs are brought out on the planar board on which the chips are mounted. The technique disclosed by J. Carson works at the chip level rather than the wafer level and thus does not reduce path lengths within the chip. Since chips are only interconnected at the outsides of the chips in the aforementioned disclosure, the wiring limitations due to on-chip delays continue to remain a potential problem. Additional work related to three-dimensional integration using laser-recrystallization or seeded-growth silicon-on-insulator technology has been described by K. Yamazaki, et al., "4-Layer 3D IC technologies for parallel signal processing," Tech. Dig. of IDEM, p. 599 (1990); K. Kioi, et al., "Design and Implementation of a 3D-LSI Character Recognition Image Sensor," Tech. Dig. of IEDM, p. 279 (1990); T. Kunio, et al., "Three dimensional ICs, having four stacked active device layers," Tech. Dig. of IEDM, p. 837 (1989); and Y. Inoue, et al., "4 PMOS/2 NMOS vertically stacked CMOS-SRAM with 0.6 μm design rule," Tech. Dig. of VSLI Technology Symposium, p. 39 (1990).

The disclosure of K. Yamazaki, et al. relates to an image processor fabricated over four silicon-on-insulator (SOI) layers that are grown by seeded overgrowth techniques. This technique requires metallurgy and devices to withstand the process conditions employed for overgrowth. Normally this necessitates device geometries that are relaxed compared to those currently utilized in the silicon industry.

The disclosure of K. Kioi, et al. reports a similar SOI technique of growing single-crystal silicon using laser irradiation for recrystallization in order to place an imaging sensor and transistor circuits on different layers. The paper authored by T. Kunio, et al. also uses laser recrystallization in order to fabricate CMOS devices on multiple layers. Y. Inoune, et al. describes the use of single-crystal and poly-crystal mixed transistors to form circuits over two layers.

In the disclosures of K. Yamazaki, et al., K. Kioi, et al., T. Kunio, et al. and Inoue, et al., short distance interconnects are described. Despite this disclosure, these references employ methods where processing is performed sequentially and requires compromises with the device in order to be compatible with the specific SOI technology.

There is thus a need for developing a new and improved method wherein integration can be achieved between processed wafers. This method would allow for short wiring (less than a mm) and wide buses to be achieved. Such a method would also provide a solution to the problem of wide data bandwidth communication between circuits, of achieving higher levels of integration, and of integration of circuits with differing processing needs while maintaining an increased manufacturing rate.

SUMMARY OF THE INVENTION

One object of the present invention is to provide a method of interconnecting circuits on more than one wafer through high-density, sub-mm length wiring.

Another object of the present invention is to allow for interconnection of active and passive elements fabricated using dissimilar technologies.

A further object of the present invention is to provide a means for forming interconnects that allow for very high electronic speeds. An additional object of the instant invention is to improve the throughput of integrated circuits.

These as well as other objects are achieved in the present invention by utilizing electro- or electroless plated wires (micro-posts) that are formed within etched insulator-walled channels in silicon wafers and interconnecting wafers using these micro-posts. Specifically, the method of the present invention comprises the step of:

(a) etching at least one hole defined by a wall and a channel at least partly through a wafer of a semiconductor material;

(b) forming a layer of electrically insulating material to cover said wall; and

(c) forming an electrically conductive material on said covered wall within said channel of the hole.

In one embodiment of the method of the present invention, the holes are etched partly through the wafer and then the opposite surface of the wafer is ground away so as to cause the holes to pass entirely through the wafer.

In another embodiment of the present invention, at least two wafers are stacked with at least one corresponding hole in alignment. When a stacked configuration is desirable, the method of the present invention further comprises the step of heating the stacked wafers to form an electrical connection between the conducting material and the corresponding holes.

In yet another embodiment of the method of the present invention, a matrix of hole channels are first etched into a wafer and then the wafer is diced into individual chip elements of the matrix.